In the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1. (Original) A method of assembling an integrated circuit chip into a package comprising:

providing a substrate;

attaching said integrated circuit chip to said substrate;

forming a dam sound said integrated circuit chip;

covering at least one corner of said integrated circuit chip with a stress buffering material; and

thereafter coating said integrated circuit chip an all of said substrate within said dam with an encapsulation material.

2. (Original) The method according to Claim 1 wherein said integrated circuit chip is attached to said substrate by a ball grid array.

3. (Original) The method according to Claim 1 wherein said integrated circuit chip is attached to said substrate by a super ball grid array (SBGA) like structure.

4. (Original) The method according to Claim 1 wherein said encapsulation material covers said stress buffering material and wherein said stress buffering material prevents delamination of said encapsulation material at said at least one corner of said integrated circuit chip.

5. (Original) The method according to Claim 1 wherein said stress buffering material comprises an epoxy or resin.

6. (Original) The method according to Claim 1 wherein said stress buffering material has a low coefficient of thermal expansion.

7. (Original) The method according to Claim 1 wherein said integrated circuit chip contains low dielectric constant dielectric layers.

8. (Original) A method of assembling an integrated circuit chip into a package comprising:

providing a substrate;

attaching said integrated circuit chip to said substrate;

forming a dam around said integrated circuit chip;

covering at least one corner of said integrated circuit chip with a stress buffering material; and

thereafter coating said integrated circuit chip and all of said substrate within said dam with an encapsulation material wherein said encapsulation material covers said stress buffering material and wherein said stress buffering material prevents delamination of said encapsulation material at said at least one corner of said integrated circuit chip.

9. (Original) The method according to Claim 8 wherein said integrated circuit chip is attached to said substrate by a ball grid array.

10. (Original) The method according to Claim 8 wherein said integrated circuit chip is attached to said substrate by a super ball grid array (SBGA) like structure.

11. (Original) The method according to Claim 8 wherein said stress buffering material comprises an epoxy or resin.

12. (Original) The method according to Claim 8 wherein said stress buffering material has a low coefficient of thermal expansion.

13. (Original) The method according to Claim 8 wherein said integrated circuit chip contains low dielectric constant dielectric layers.

14. (Original) An integrated circuit chip package comprising:

an integrated circuit chip attached to a substrate;

a dam surrounding said integrated circuit chip;

a stress buffering material covering at least one corners of said integrated circuit chip; and

an encapsulation material coating said integrated circuit chip and all of said substrate within said dam.

15. (Original) The package according to Claim 14 wherein said integrated circuit chip is attached to said substrate by a ball grid array.

16. (Original) The package according to Claim 14 wherein said integrated circuit chip is attached to said substrate by a super ball grid array (SBGA) like structure.

17. (Original) The package according to Claim 14 wherein said encapsulation material covers said stress buffering material and wherein said stress buffering material prevents delamination of said encapsulation material at said at least one corner of said integrated circuit chip.

18. (Original) The package according to Claim 14 wherein said stress buffering material comprises an epoxy or resin.

19. (Original) The package according to Claim 14 wherein said stress buffering material has a low coefficient of thermal expansion.

20. (Original) The package according to Claim 14 wherein said integrated circuit chip contains low dielectric constant dielectric layers.